REMARKS

This paper is in response to the Office Action of January 13, 2005. A two month extension is hereby petitioned for, extending the period of response to June 13, 2005.

New formal drawings are enclosed, and are marked as Replacement Sheets.

The Examiner rejected claims 1-5, 9, 10, and 12-18 and 20-25 under 35 USC § 102(b) over Krishnamurthy (USP 6,271,713). Claims 12 -19 were rejected under 35 USC § 102 (b) over Taylor (USP 5,644,255). Claims 1-19 were cancelled, and thus the rejection over Taylor is moot.

Claims 11-25 have been cancelled. Accordingly, the Section 112 rejections are now rendered moot.

The Applicants have reviewed the cited art and have made amendments to the remaining claims to emphasize the differences between the now claimed invention and the teachings of the cited art. With reference to Krishnamurthy, the teaching is to provide a balanced driver circuit. The driver circuit is defined by a double inverter buffer bypassed with a pull-up n-channel field effect transistor (nFET). An important consideration for Krishnamurthy is to achieve high speed drive, and the drive is achieved by using two identical inverters. For instance, the inventors 152/154 of Figure 4 and the inverters 162/164 of Figure 5 are identical. Further, the bias voltage Vdd (116) applied to the P-type transistors M2/M4 and N-type transistor M1 is identical. This arrangement is required to achieve the correct drive speed in a driver circuit configuration.

Independent claim 1 has been amended to emphasize the transistor and voltage level configuration implemented when the circuit is used to communicate signals between two different transistor and voltage level regions. As noted, one implementation of the present invention is to transition between an I/O ring region and a core region. Transistors in the I/O ring region are generally larger than those in the core. Also, the voltage level (Vdd) in the I/O region is higher than in the core. But, when transitions occur, the inverting circuit is different, as it is defined using I/O ring larger transistors. These larger I/O ring transistors,

however, are operated using a lower core voltage level Vdd. This structural configuration is now claimed.

Krishnamurthy is completely silent on the functionally or structure for transitioning from a first voltage level to a second voltage level. The structure disclosed and taught by Krishnamurthy is have all transistors in both inventors the same. Also, the voltage levels applied to both inverters are identical (i.e., Vdd 116). Modification away from the clear teachings of Krishnamurthy would not be contemplated by one skilled in the art, as such modification is contrary to having a uniform drive circuit with identical transistor inventor pairs, powered by the same Vdd. In view of the foregoing, the Applicants respectfully submit that Krishnamurthy fails to teach or make the now claimed invention obvious. Withdrawal of this rejection is respectfully requested.

New claims 26-28 have been added to further define the first voltage level, the second voltage level, the first size transistors and the second size transistors. No new matter was introduced by these definitions, which are supported by the as-filed specification and drawings.

If the Examiner has any questions concerning the present amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6903. If any other fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No ARTCP043). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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